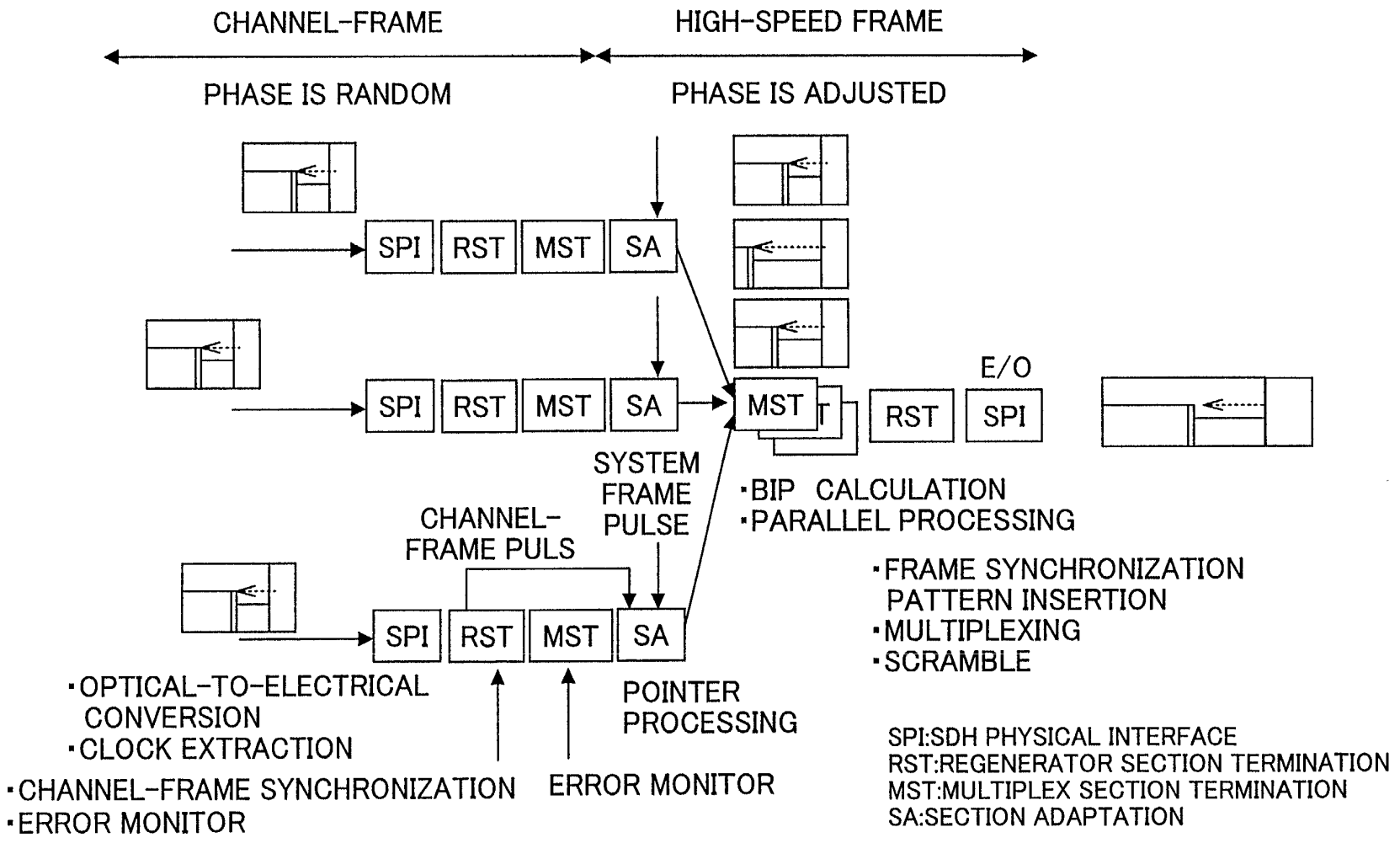
T05T90"h2E28860

FIG.1 PRIOR ART



TOSTSD"h2E28860

FIG.2 PRIOR ART

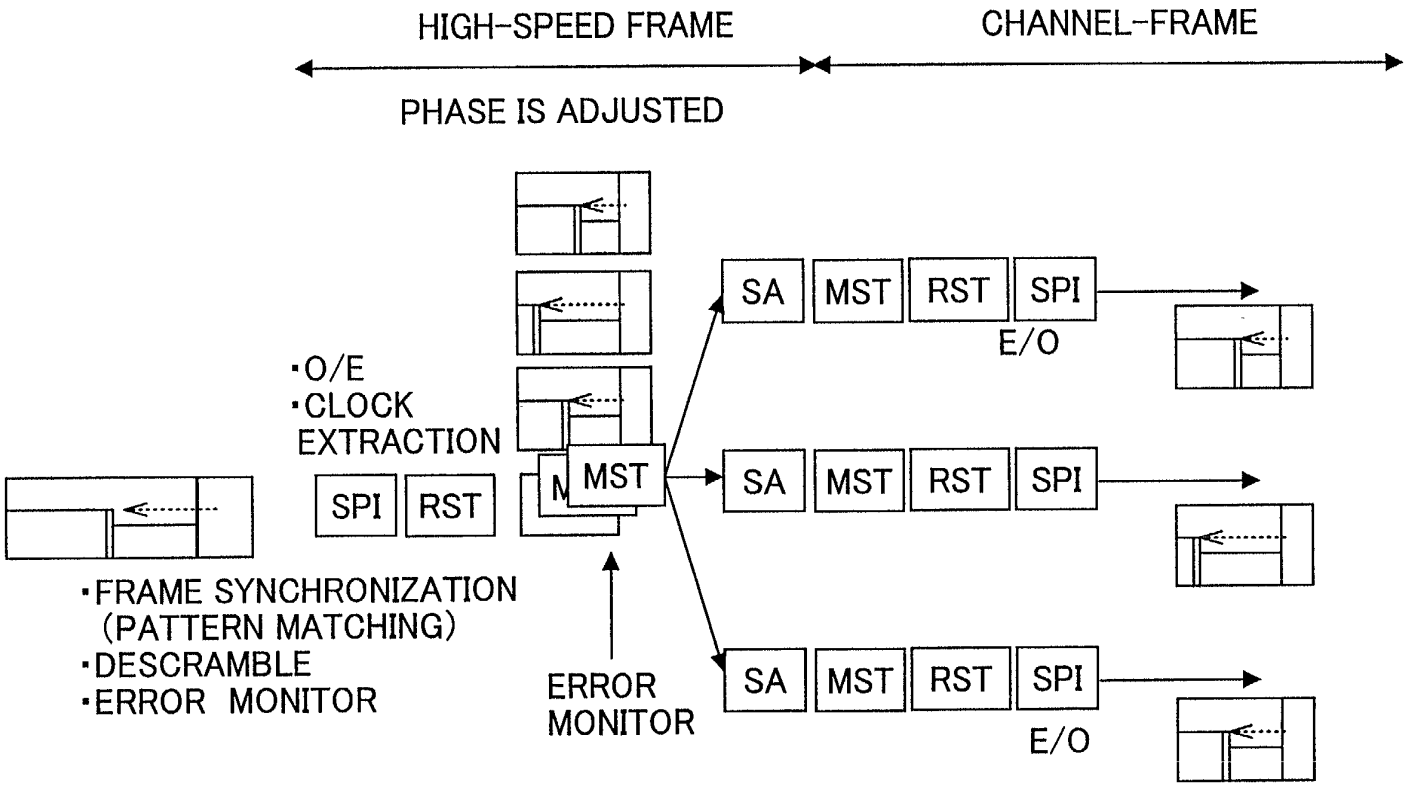
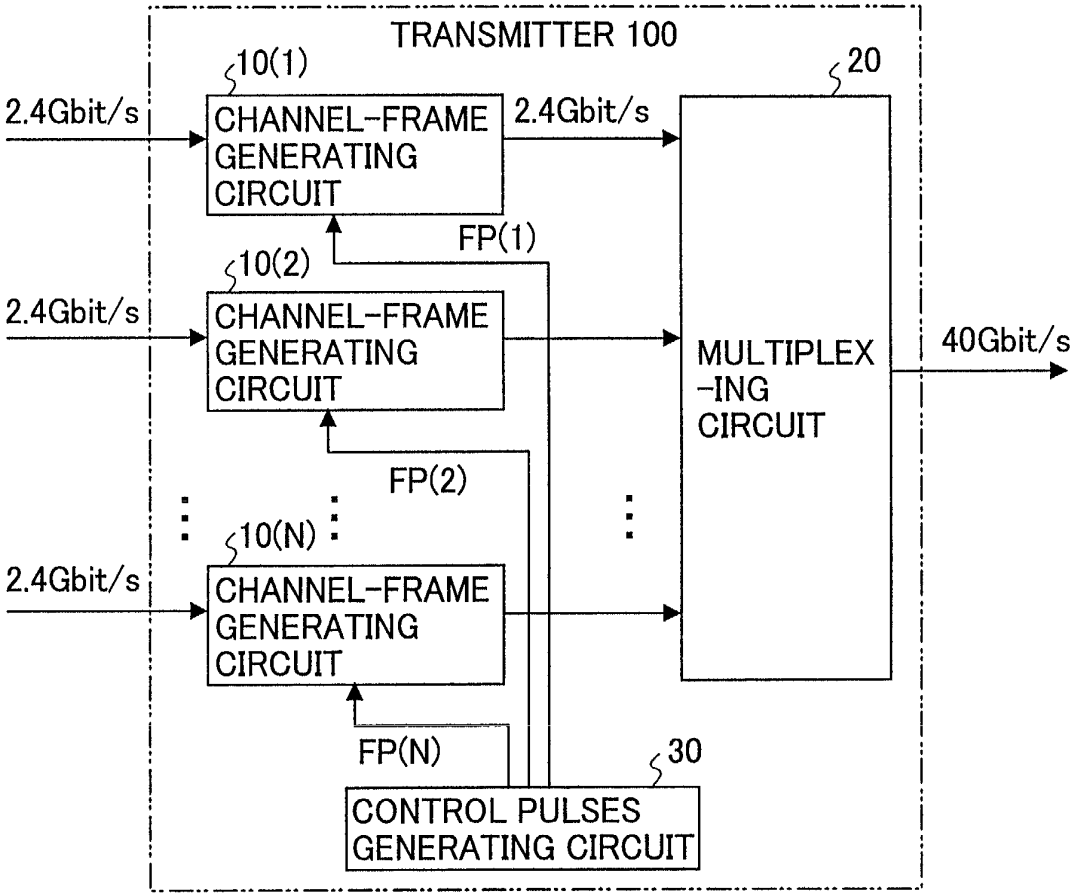
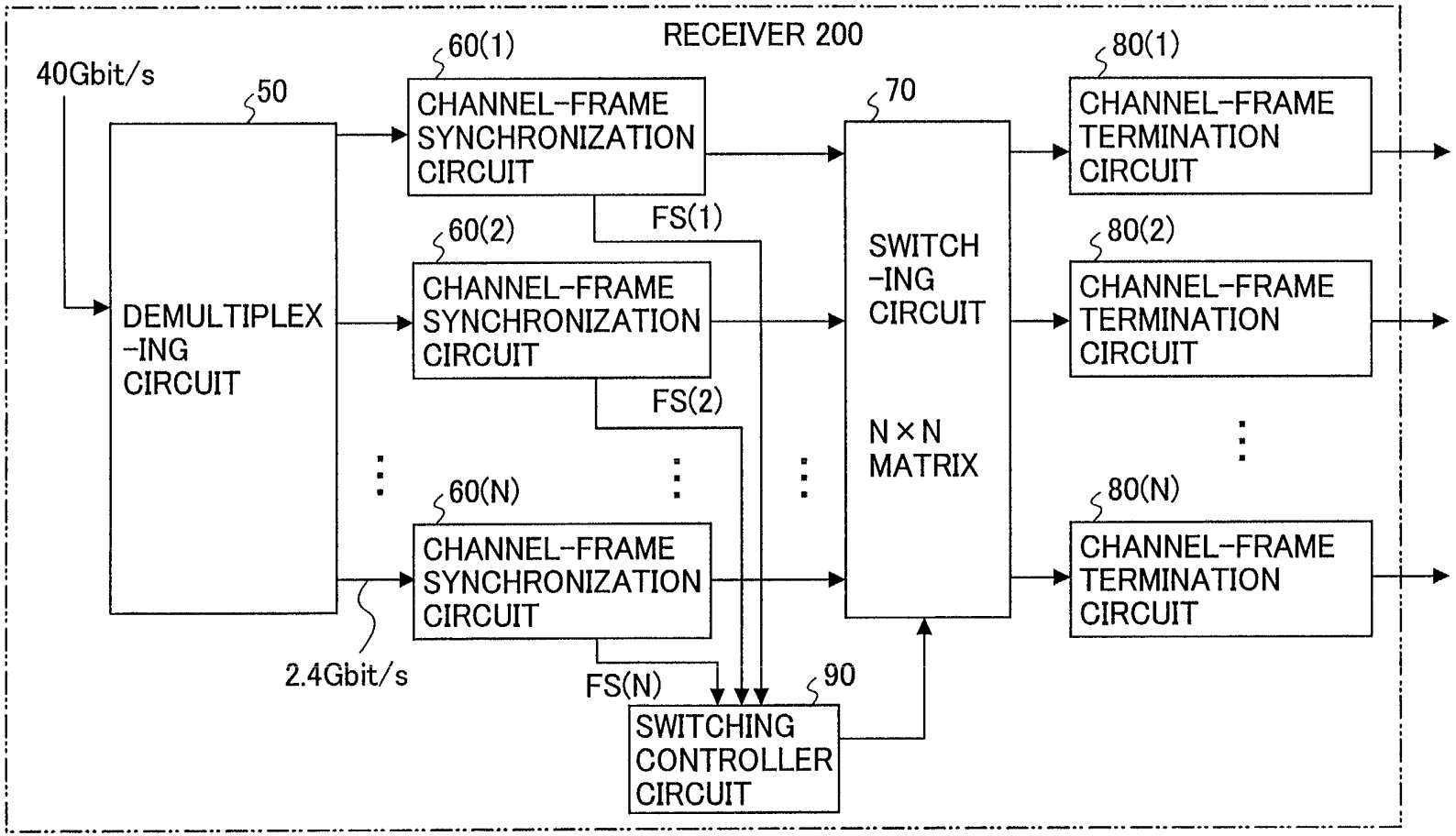


FIG.3A


TRANSMITTER 100
10(1)
20
2.4Gbit/s
CHANNEL-FRAME GENERATING CIRCUIT
2.4Gbit/s
FP(1)
10(2)
2.4Gbit/s
CHANNEL-FRAME GENERATING CIRCUIT
MULTIPLEX -ING CIRCUIT
40Gbit/s
FP(2)
10(N)
2.4Gbit/s
CHANNEL-FRAME GENERATING CIRCUIT
FP(N)
30
CONTROL PULSES GENERATING CIRCUIT

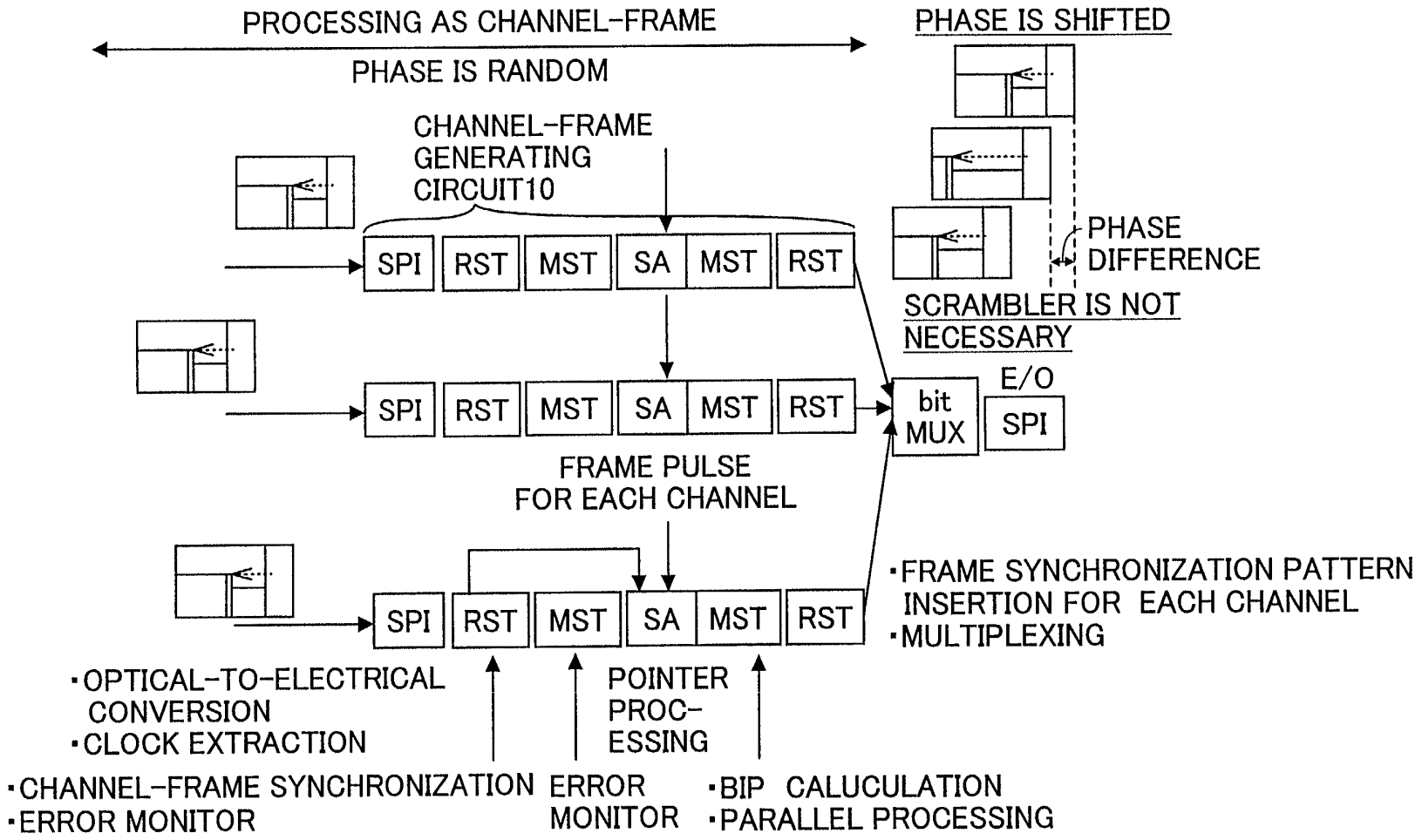
TOSTSO"h2E28860

FIG.3B



JP2003060860

FIG.4



TOSTSO"h2E39360

FIG.5

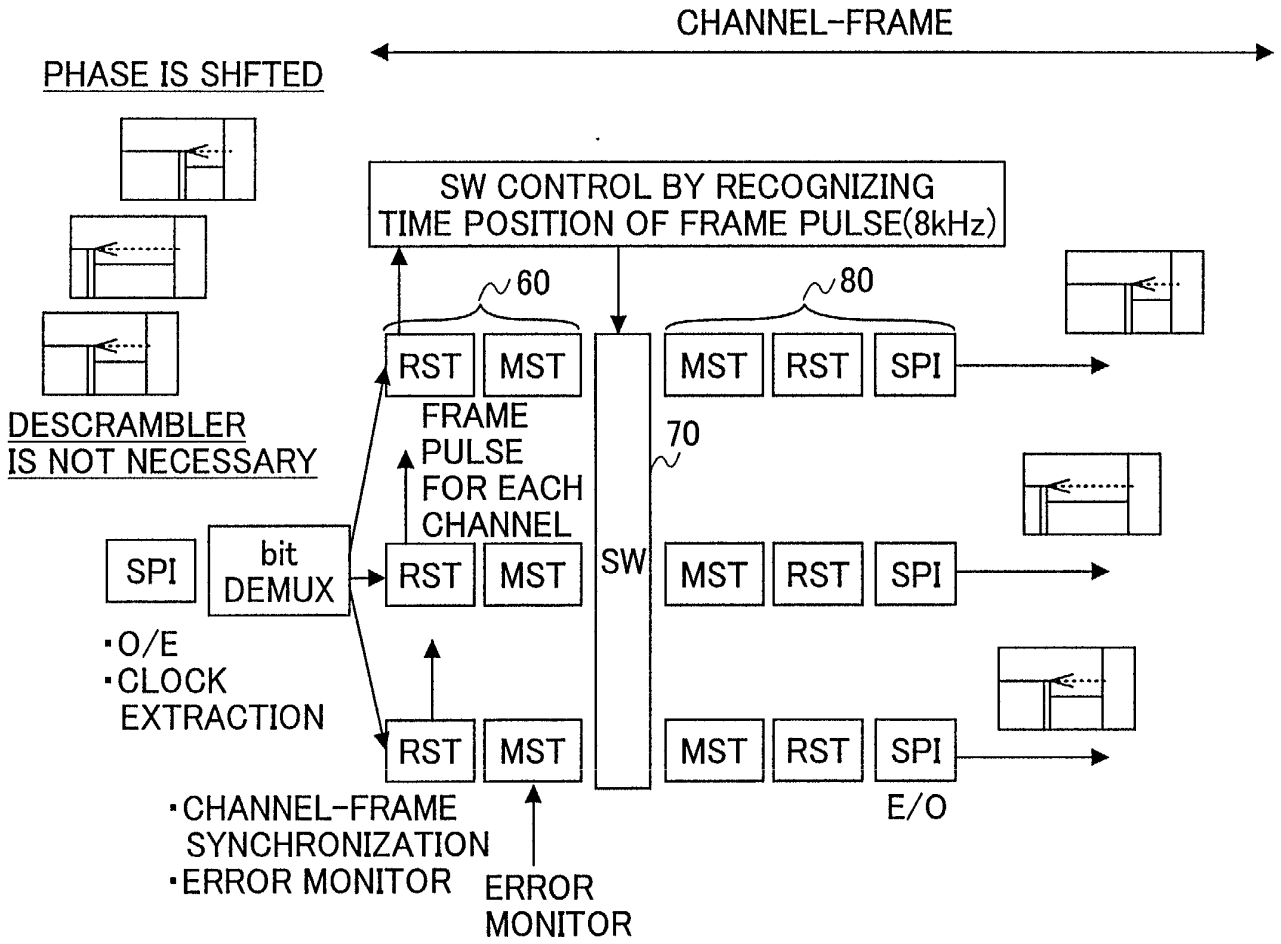


FIG.6A

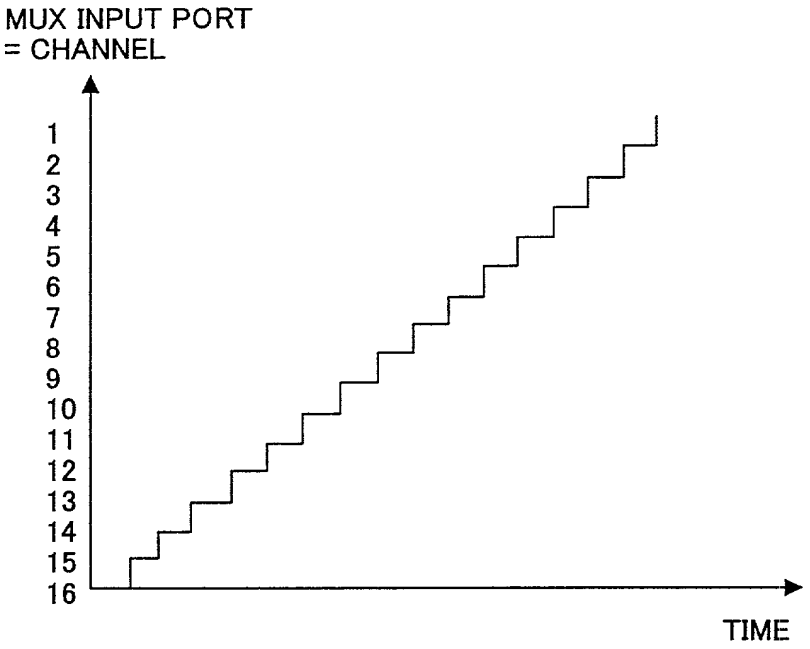

MUX INPUT PORT
= CHANNEL
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
TIME

FIG.6B

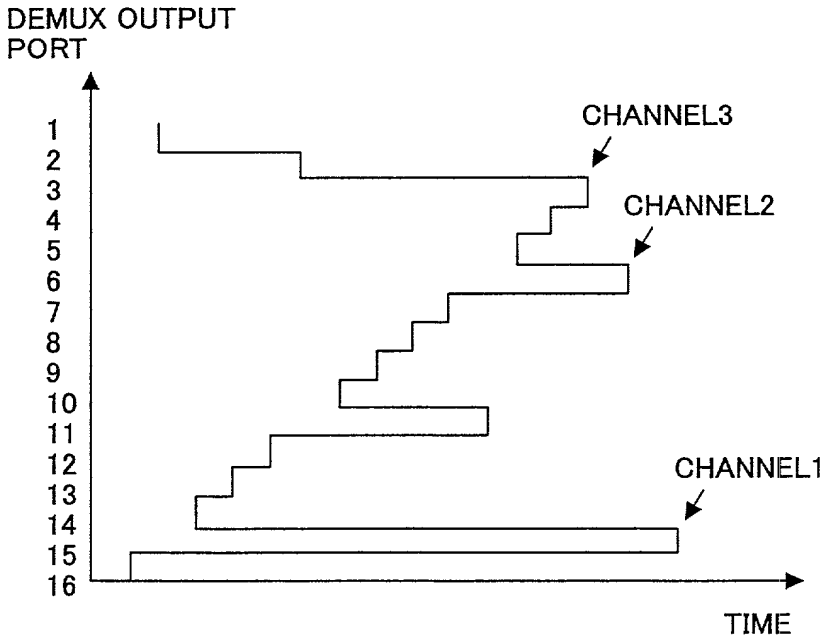
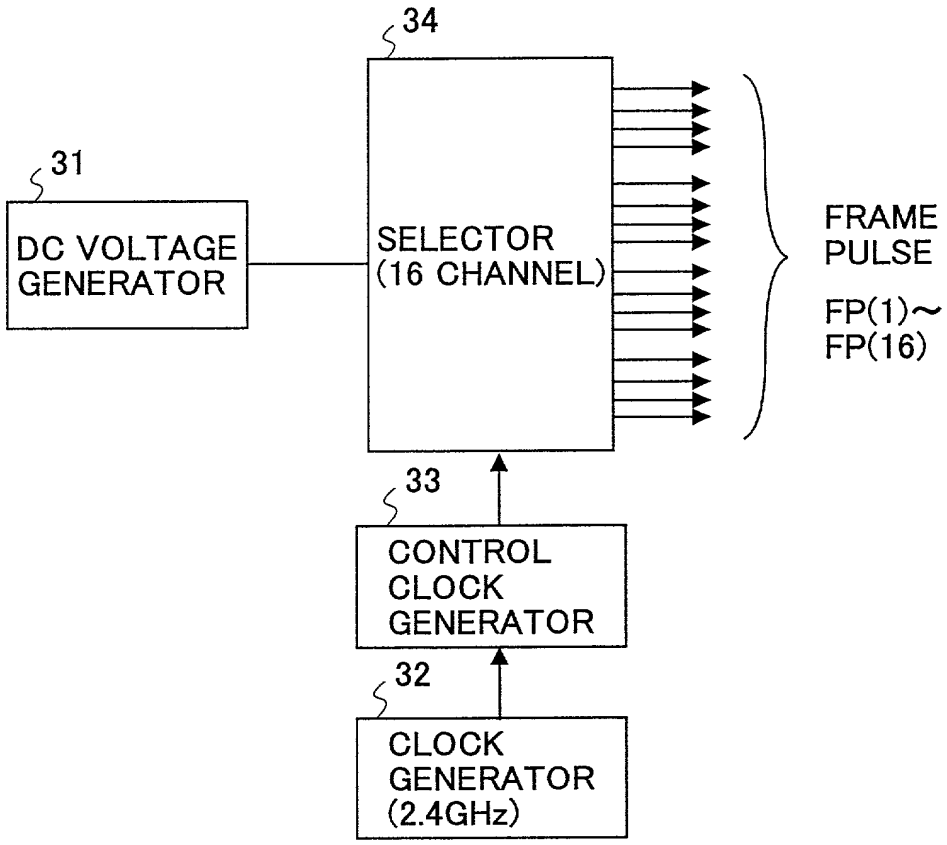
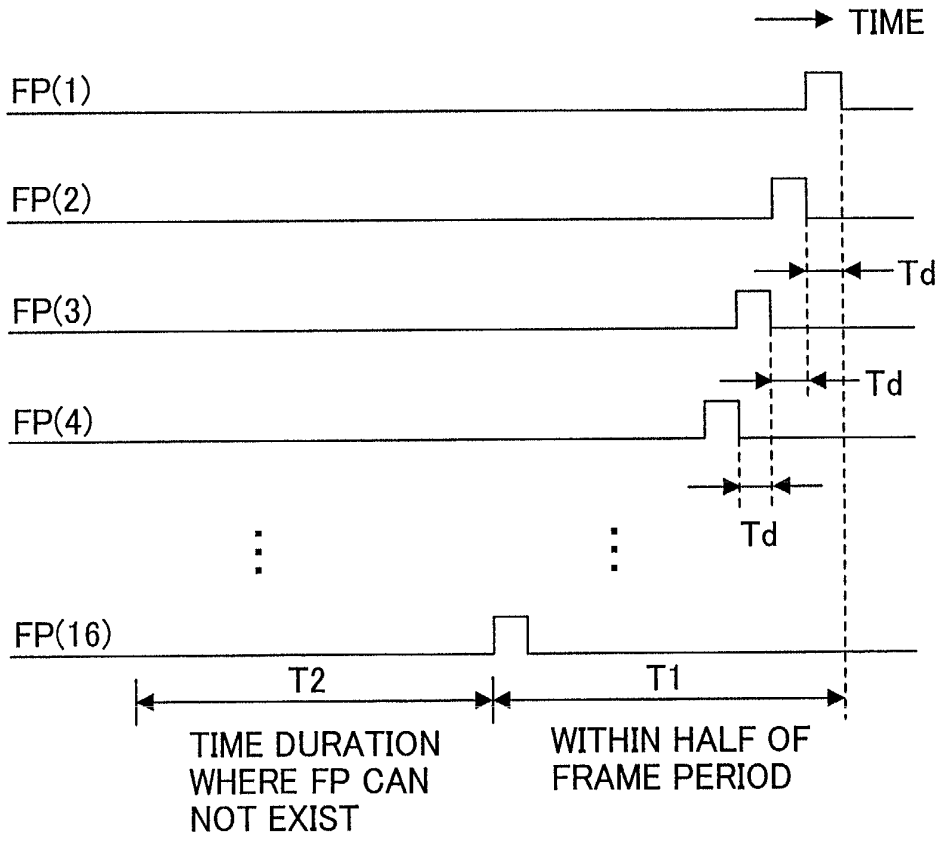

DEMUX OUTPUT
PORT
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
CHANNEL3
CHANNEL2
CHANNEL1
TIME

FIG.7


34
31
DC VOLTAGE GENERATOR
SELECTOR (16 CHANNEL)
FRAME PULSE
FP(1)～ FP(16)
33
CONTROL CLOCK GENERATOR
32
CLOCK GENERATOR (2.4GHz)

TOSTSO"hEE28860

FIG.8



JP 2008-028860

FIG.9

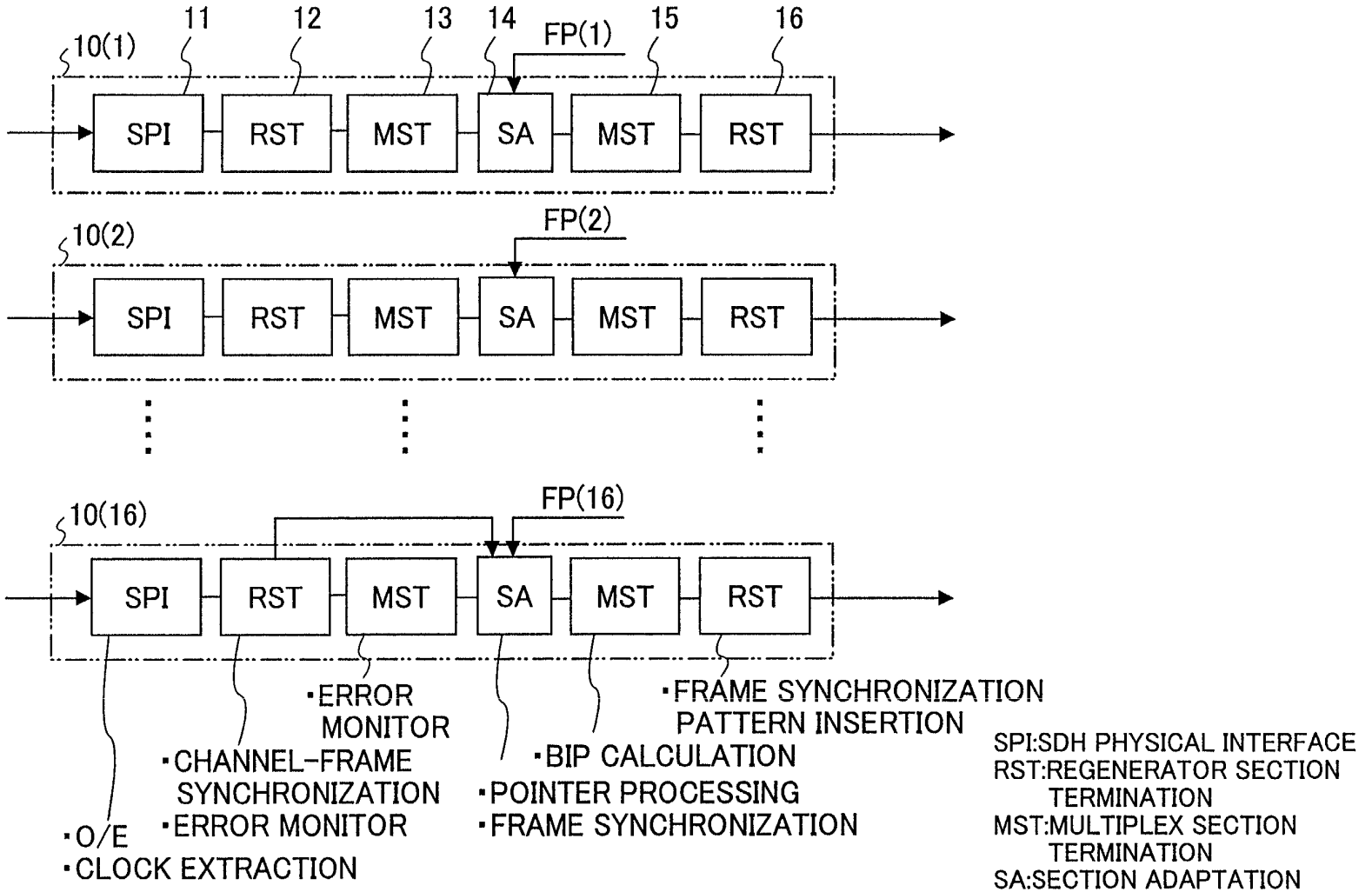


FIG.10

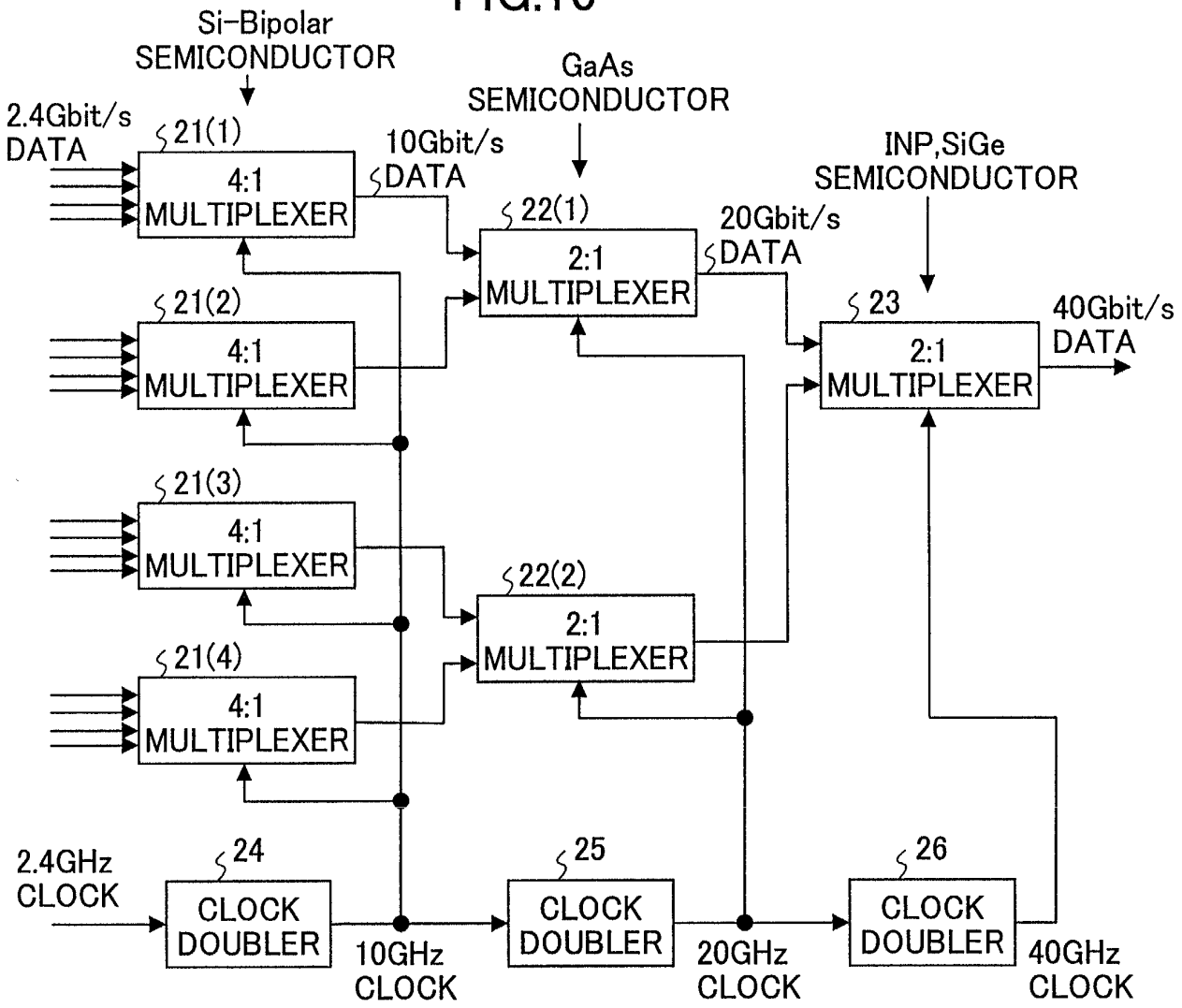
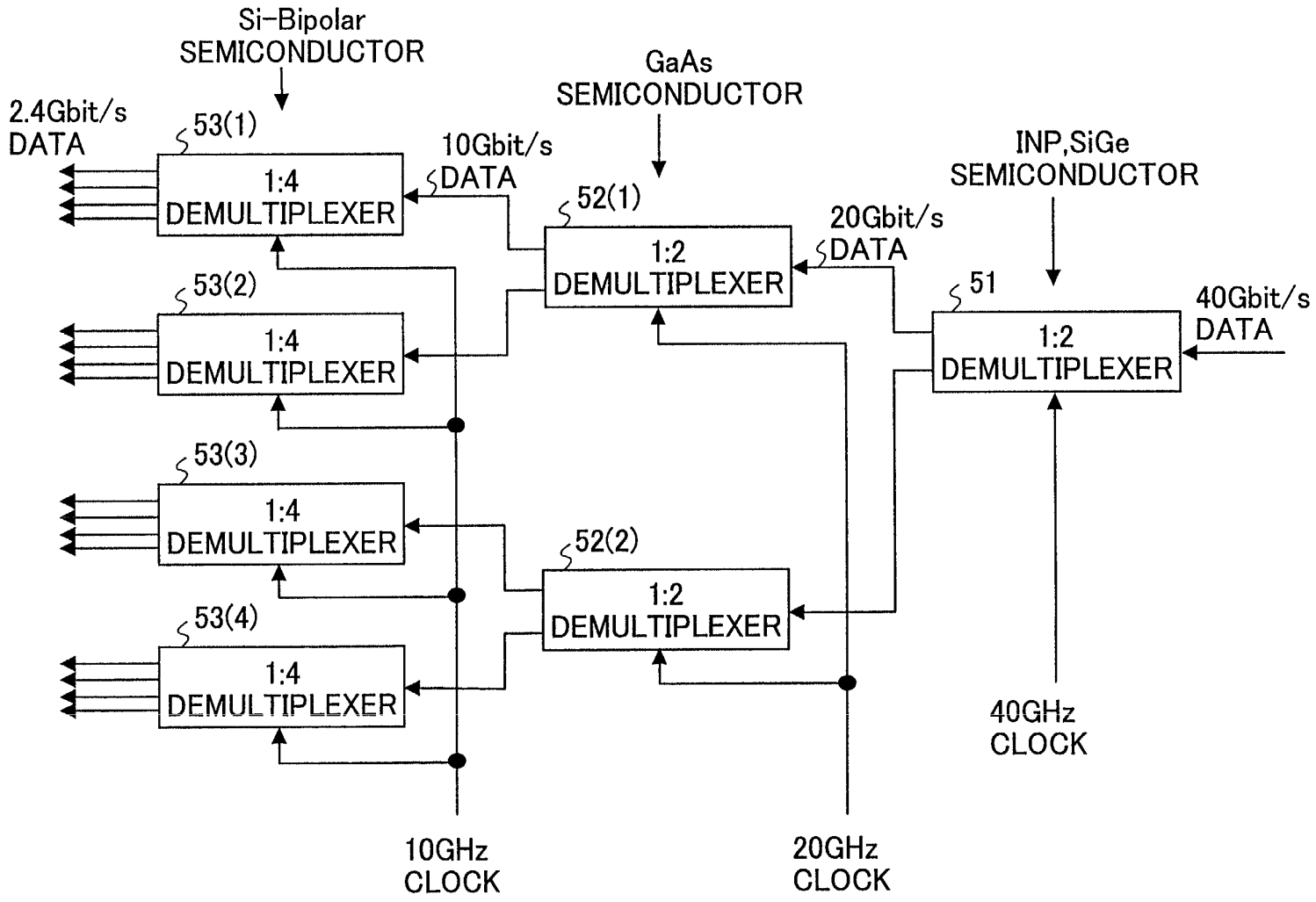

Si-Bipolar
SEMICONDUCTOR
GaAs
SEMICONDUCTOR
INP,SiGe
SEMICONDUCTOR
2.4Gbit/s
DATA
21(1)
4:1
MULTIPLEXER
10Gbit/s
DATA
22(1)
2:1
MULTIPLEXER
20Gbit/s
DATA
23
2:1
MULTIPLEXER
40Gbit/s
DATA
21(2)
4:1
MULTIPLEXER
21(3)
4:1
MULTIPLEXER
22(2)
2:1
MULTIPLEXER
21(4)
4:1
MULTIPLEXER
2.4GHz
CLOCK
24
CLOCK
DOUBLER
10GHz
CLOCK
25
CLOCK
DOUBLER
20GHz
CLOCK
26
CLOCK
DOUBLER
40GHz
CLOCK

FIG.11


Si-Bipolar
SEMICONDUCTOR
GaAs
SEMICONDUCTOR
INP,SiGe
SEMICONDUCTOR
2.4Gbit/s
DATA
53(1)
1:4
DEMULTIPLEXER
10Gbit/s
DATA
52(1)
1:2
DEMULTIPLEXER
20Gbit/s
DATA
51
1:2
DEMULTIPLEXER
40Gbit/s
DATA
53(2)
1:4
DEMULTIPLEXER
53(3)
1:4
DEMULTIPLEXER
52(2)
1:2
DEMULTIPLEXER
53(4)
1:4
DEMULTIPLEXER
40GHz
CLOCK
10GHz
CLOCK
20GHz
CLOCK

TOSTSO"h2E28860

FIG.12

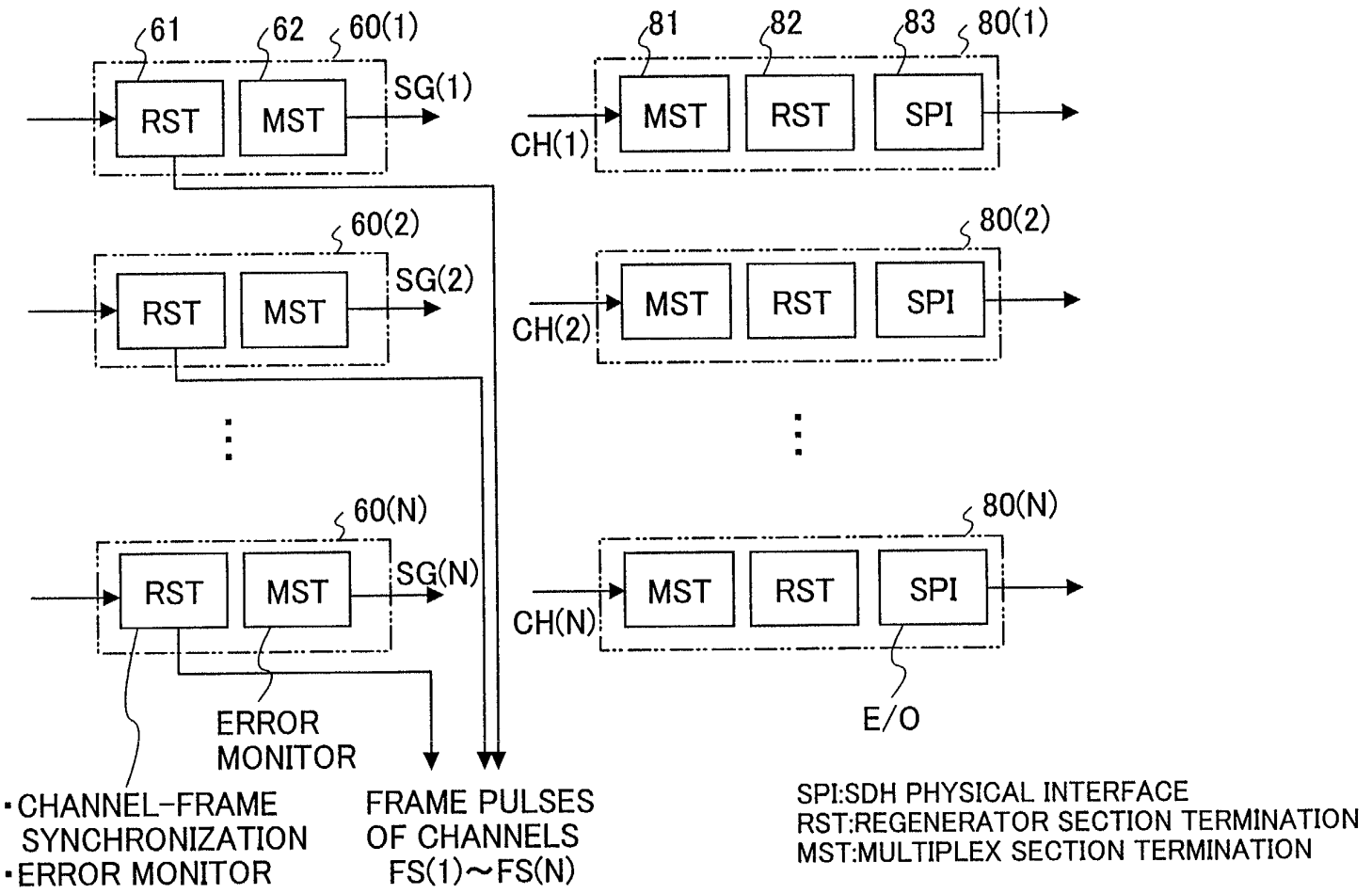


FIG.13

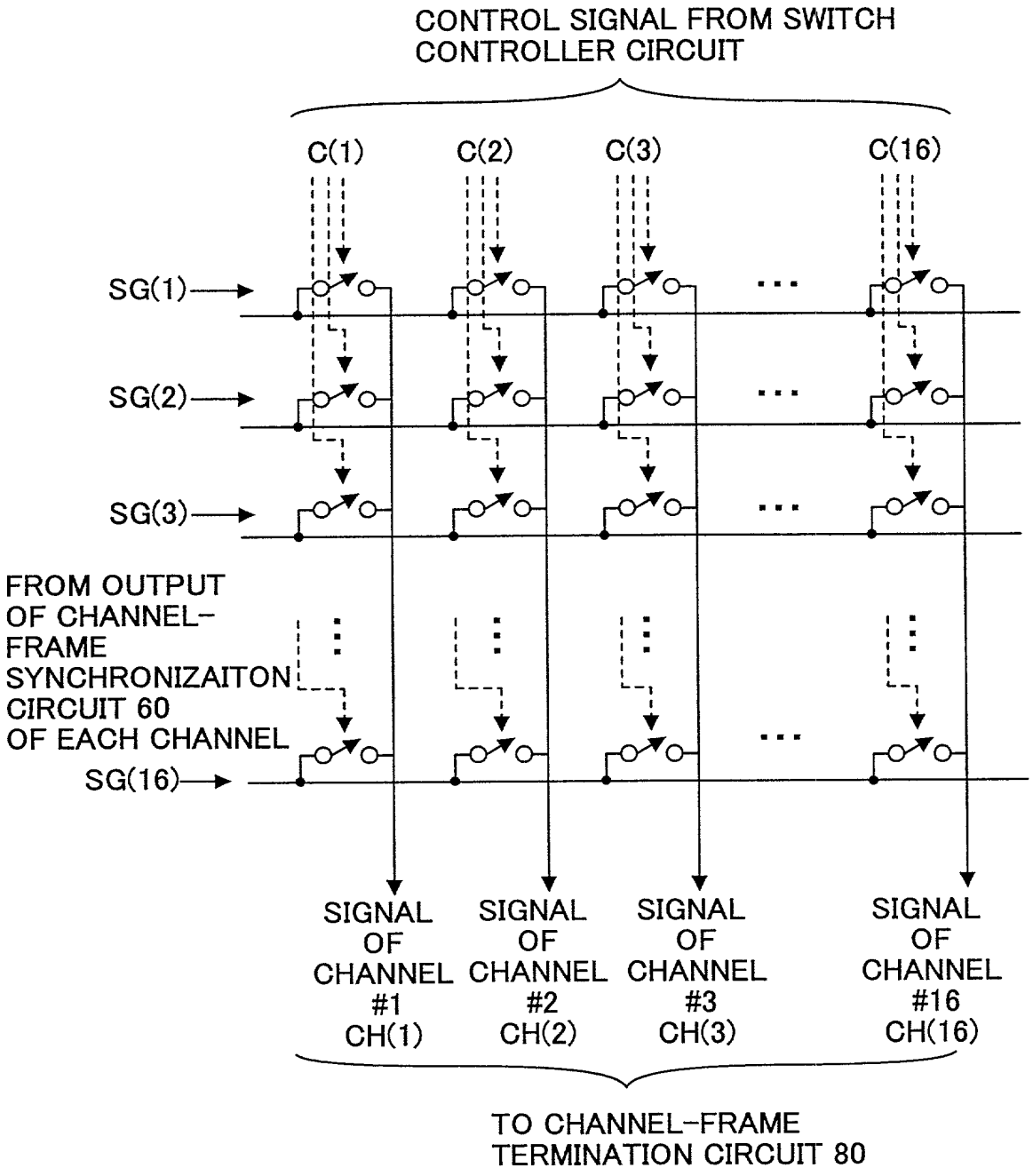

CONTROL SIGNAL FROM SWITCH CONTROLLER CIRCUIT
C(1)
C(2)
C(3)
C(16)
SG(1)
SG(2)
SG(3)
SG(16)
FROM OUTPUT OF CHANNEL-FRAME SYNCHRONIZAITON CIRCUIT 60 OF EACH CHANNEL
SIGNAL OF CHANNEL #1 CH(1)
SIGNAL OF CHANNEL #2 CH(2)
SIGNAL OF CHANNEL #3 CH(3)
SIGNAL OF CHANNEL #16 CH(16)
TO CHANNEL-FRAME TERMINATION CIRCUIT 80

FIG.14

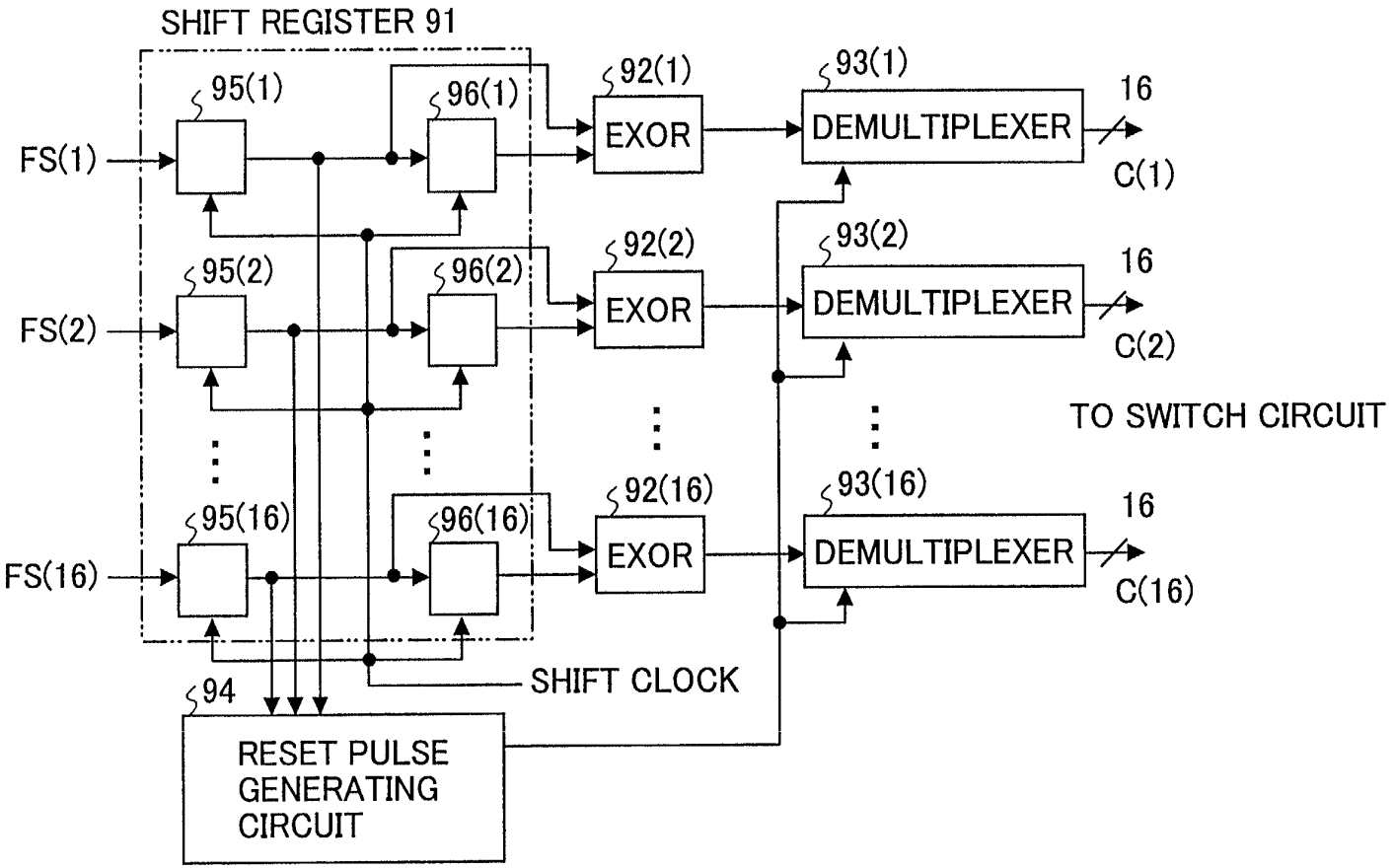

SHIFT REGISTER 91
95(1)
96(1)
92(1)
93(1)
EXOR
DEMULTIPLEXER
16
C(1)
FS(1)
95(2)
96(2)
92(2)
93(2)
EXOR
DEMULTIPLEXER
16
C(2)
FS(2)
TO SWITCH CIRCUIT
95(16)
96(16)
92(16)
93(16)
EXOR
DEMULTIPLEXER
16
C(16)
FS(16)
SHIFT CLOCK
94
RESET PULSE GENERATING CIRCUIT

FIG.15A

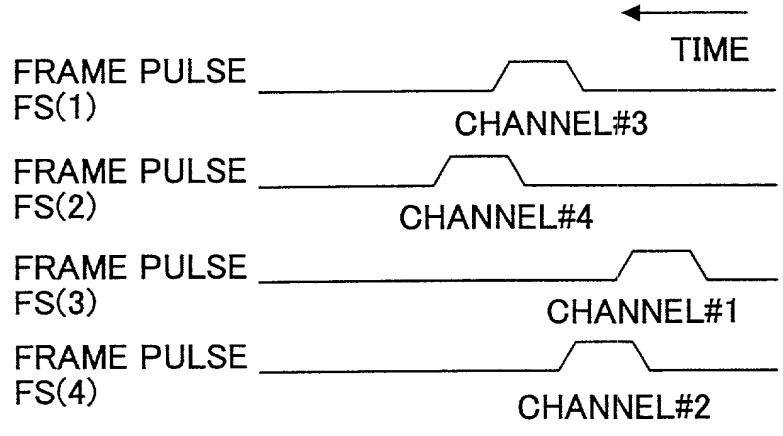


FIG.15B

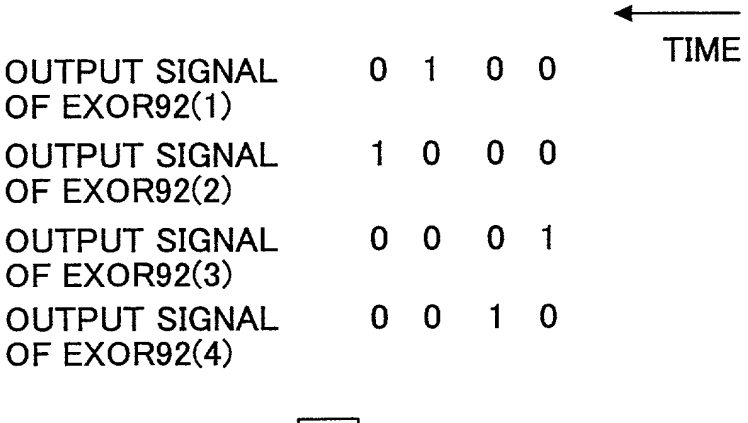


FIG.15C

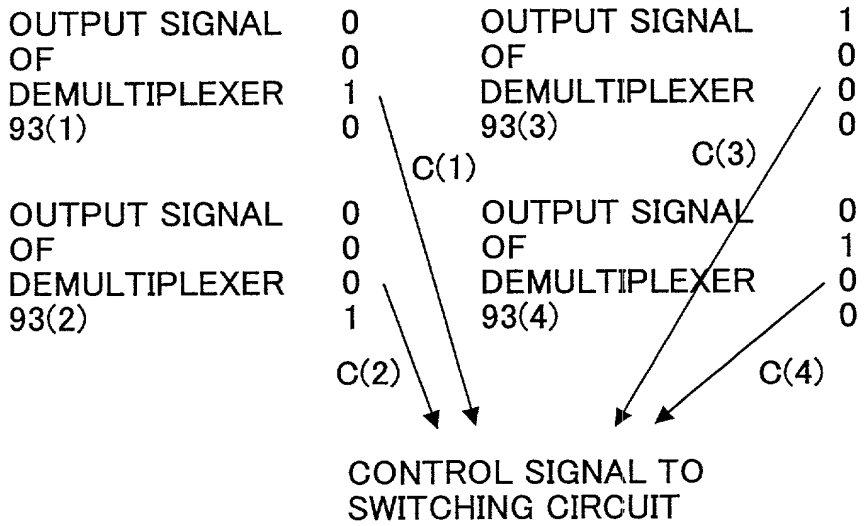
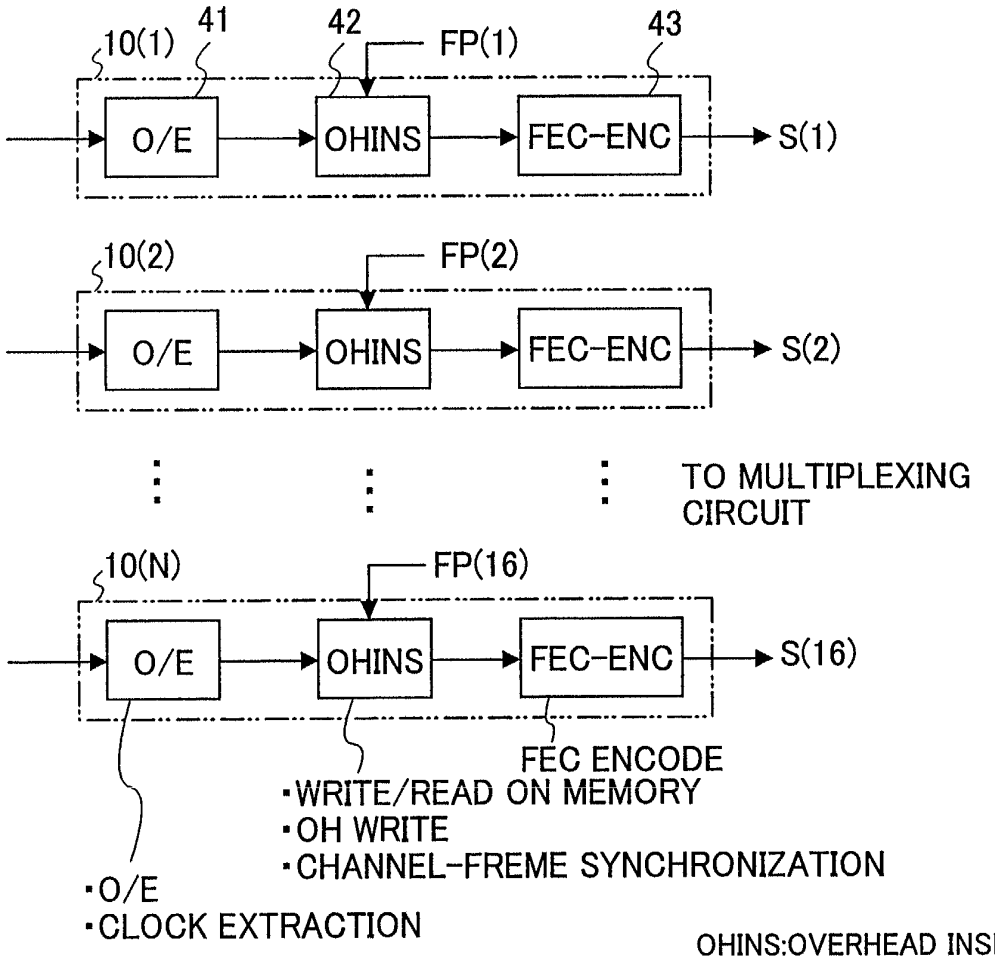


FIG.16



OHINS:OVERHEAD INSERTION CIRCUIT
FEC-ENC:FORWARD ERROR CORRECTION-ENCODER

FIG.17

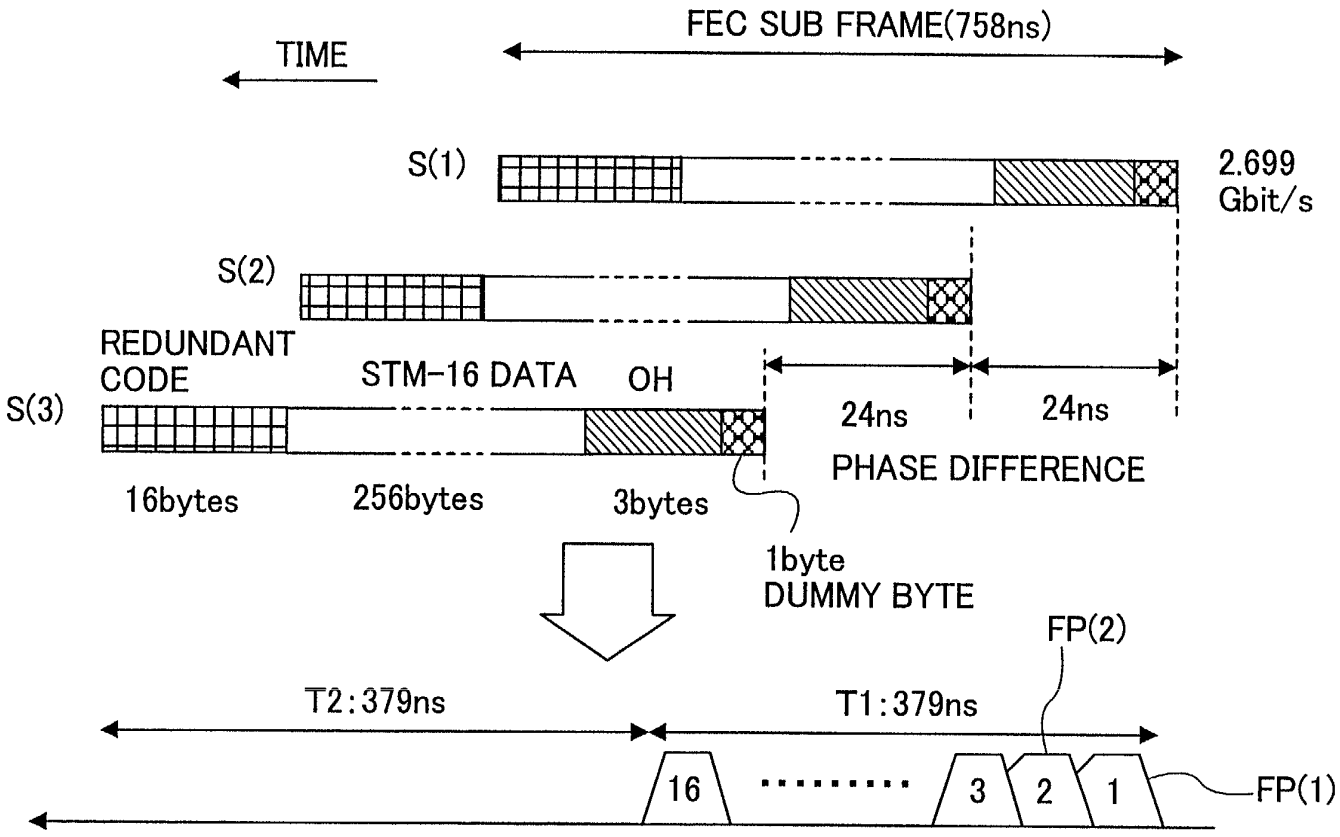

TIME
FEC SUB FRAME(758ns)
S(1)
2.699
Gbit/s
S(2)
REDUNDANT
CODE
STM-16 DATA
OH
S(3)
24ns
24ns
PHASE DIFFERENCE
16bytes
256bytes
3bytes
1byte
DUMMY BYTE
FP(2)
T2:379ns
T1:379ns
16
3
2
1
FP(1)

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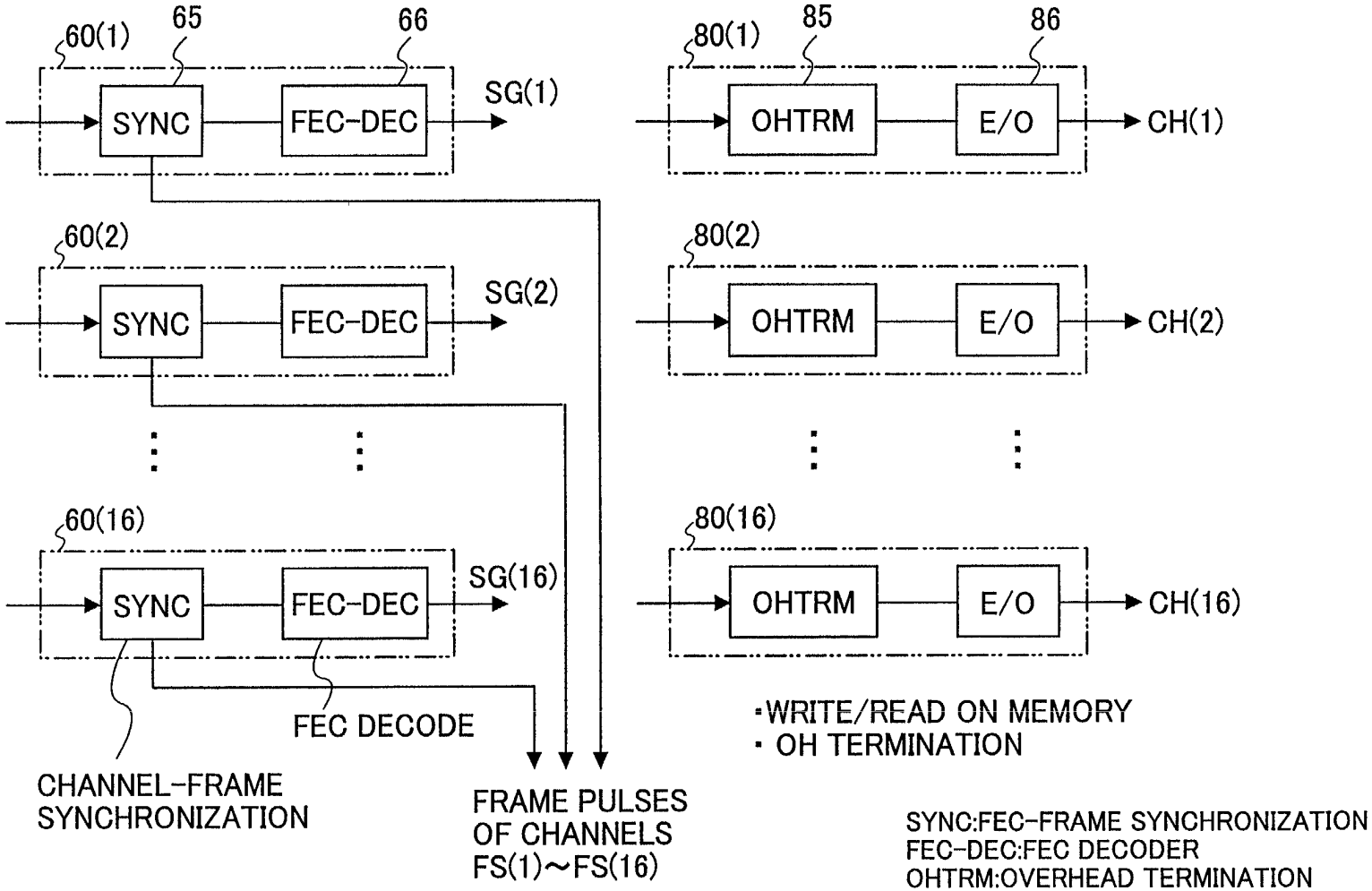
FIG.18



TOSTSO"hZE28860

FIG.19

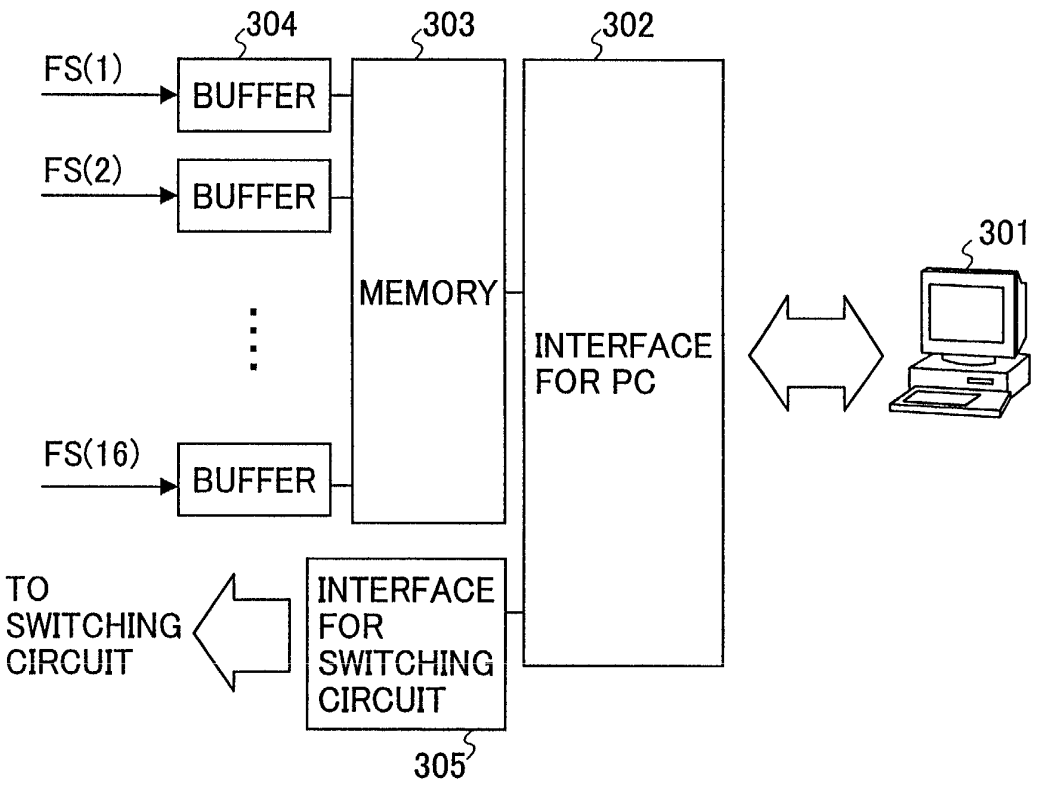
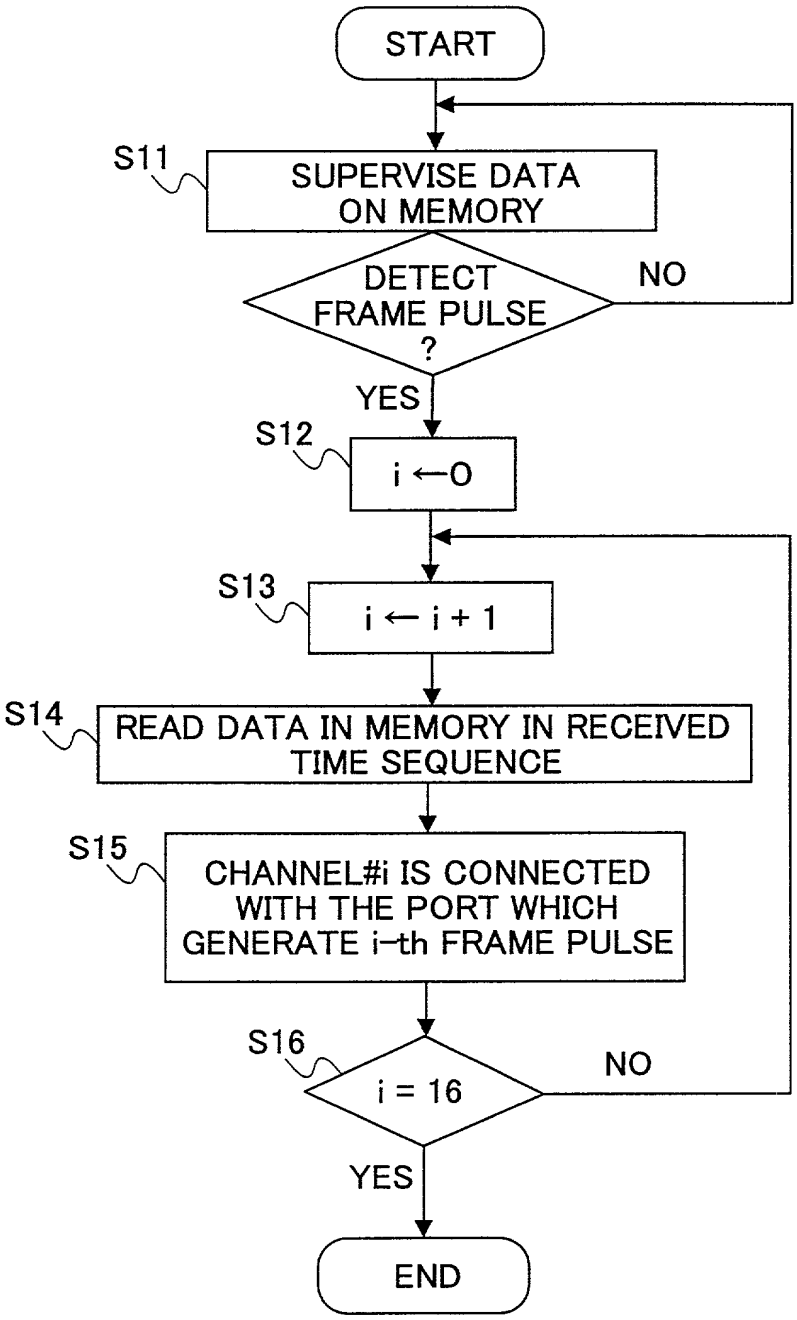


FIG.20


START
S11
SUPERVISE DATA ON MEMORY
DETECT FRAME PULSE ?
NO
YES
S12
i ←0
S13
i ← i + 1
S14
READ DATA IN MEMORY IN RECEIVED TIME SEQUENCE
S15
CHANNEL#i IS CONNECTED WITH THE PORT WHICH GENERATE i-th FRAME PULSE
S16
i = 16
NO
YES
END